IN THE CLAIMS:

Claims 1 and 19 have been cancelled and claims 3 and 21 have been amended herein. Additionally, claims 2, 11 through 18 and 20, which claims have been previously withdrawn, have been cancelled herein. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1 and 2 (cancelled)

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Claim 3 (currently amended) A transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer planarized down to said at least one transistor gate member and substantially covering said at least one thick field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one source region on said semiconductor substrate;

an individual drain contact land disposed atop each of said at least one drain contact plugs and a portion of said first barrier layer, said individual drain contact land wider than said at least one drain contact plug ~~and substantially planar~~;

an individual source contact land disposed atop each of said at least one source contact plugs and a portion of said first barrier layer, said individual source contact land wider than said at least one source contact plug ~~and substantially planar~~;

a second barrier layer disposed over said first barrier layer, said individual drain contact land, and said individual source contact land;

at least one upper source contact extending through said second barrier layer, said at least one upper source contact in electrical communication with at least one of said individual source contact lands; and

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at least one upper drain contact extending through said second barrier layer, said at least one upper drain contact in electrical communication with at least one of said individual drain contact lands.

Claim 4 (previously presented) The transistor of claim 3, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

Claim 5 (previously presented) The transistor of claim 3, wherein said at least one source contact plug extends between at least two source regions.

Claim 6 (previously presented) The transistor of claim 3, wherein said at least one drain contact plug extends between at least two drain regions.

Claim 7 and 8 (canceled)

Claim 9 (previously presented) The transistor of claim 3, wherein said at least one upper source contact extends between at least two individual source contact lands.

Claim 10 (previously presented) The transistor of claim 3, wherein said at least one upper drain contact extends between at least two individual drain contact lands.

Claims 11 through 18 (Previously Withdrawn and Cancelled Herein)

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Claims 19 and 20 (canceled)

Claim 21 (currently amended) A semiconductor device including at least one transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer planarized down to said at least one transistor gate member and substantially covering said at least one thick field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one implanted drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one implanted source region on said semiconductor substrate;

an individual drain contact land disposed atop said at least one drain contact plug and a portion of said first barrier layer, said individual drain contact land wider than said at least one drain contact plug ~~and substantially planar~~;

an individual source contact land disposed atop said at least one source contact plug and a portion of said first barrier layer, said individual source contact land wider than said at least one source contact plug ~~and substantially planar~~;

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a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, said at least one upper source contact in electrical communication with at least one said individual source contact land; and

at least one upper drain contact extending through said second barrier layer, said at least one upper drain contact in electrical communication with at least one said individual drain contact land.

Claim 22 (original) The semiconductor device of claim 21, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

Claim 23 (previously presented) The semiconductor device of claim 21, wherein said at least one source contact plug extends between at least two source regions.

Claim 24 (previously presented) The semiconductor device of claim 21, wherein said at least one drain contact plug extends between at least two drain regions.

Claims 25 and 26 (canceled)

Claim 27 (previously presented) The semiconductor device of claim 21, wherein said at least one upper source contact extends between at least two individual source contact lands.

Claim 28 (previously presented) The semiconductor device of claim 21, wherein said at

least one upper drain contact extends between at least two individual drain contact lands.

Claim 29 (previously presented) A contact for a semiconductor device, comprising:

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a single contact plug extending through a first barrier layer and a second barrier layer, said second barrier layer disposed over said first barrier layer and planarized down to a transistor gate member, said single contact plug being in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop said single contact plug and a portion of said second barrier layer, wherein said individual contact land is wider than said single contact plug;

an upper contact extending through a third barrier layer, said third barrier layer disposed over said second barrier layer, to form an electrical contact with said individual contact land.

Claim 30 (previously presented) A transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer substantially covering said at least one thick field oxide area and said at least one active area, and adjacent said at least one transistor gate member;

a second barrier layer disposed over said first barrier layer and planarized down to said at least one transistor gate member;

at least one drain contact plug extending through each of said first and second barrier layers, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through each of said first and second barrier layers, wherein said at least one source contact plug is in electrical communication with said at least one source region on said semiconductor substrate;

an individual drain contact land disposed atop each of said at least one drain contact plugs and a portion of said second barrier layer, said individual drain contact land wider than said at least one drain contact plug;

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an individual source contact land disposed atop each of said at least one source contact plugs and a portion of said second barrier layer, said individual source contact land wider than said at least one source contact plug;

a third barrier layer disposed over said second barrier layer, said individual drain contact land, and said individual source contact land;

at least one upper source contact extending through said third barrier layer, said at least one upper source contact in electrical communication with said individual source contact land; and

at least one upper drain contact extending through said third barrier layer, said at least one upper drain contact in electrical communication with said individual drain contact land.

Claim 31 (previously presented) A semiconductor device including at least one contact, comprising:

a single contact plug extending through each of a first barrier layer and a second barrier layer, said second barrier disposed over said first barrier layer and planarized down to a transistor gate member, said single contact plug being in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop said single contact plug and a portion of said second barrier layer, said individual contact land being wider than said single contact plug; and

an upper contact extending through a third barrier layer, said third barrier layer disposed over said second barrier layer, to form an electrical contact with said individual contact land.

Claim 32 (previously presented) A semiconductor device including at least one transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

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a first barrier layer substantially covering said at least one thick field oxide area and said at least one active area, and adjacent said at least one transistor gate member;

a second barrier layer disposed over said first barrier layer and planarized down to said at least one transistor gate member;

at least one drain contact plug extending through each of said first and second barrier layers, wherein said at least one drain contact plug is in electrical communication with said at least one implanted drain region on said semiconductor substrate;

at least one source contact plug extending through each of said first and second barrier layers, wherein said at least one source contact plug is in electrical communication with said at least one implanted source region on said semiconductor substrate;

an individual drain contact land disposed atop said at least one drain contact plug and a portion of said second barrier layer, said individual drain contact land being wider than said at least one drain contact plug;

an individual source contact land disposed atop said at least one source contact plug and a portion of said second barrier layer, said individual source contact land being wider than said at least one source contact plug;

a third barrier layer disposed over said second barrier layer, said individual source contact land and said individual drain contact land;

at least one upper source contact extending through said third barrier layer, said at least one upper source contact being in electrical communication with said individual source contact land; and

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at least one upper drain contact extending through said third barrier layer, said at least one upper drain contact being in electrical communication with said individual drain contact land.